WHAT IS CLAIMED IS:

1. A method for forming a high resistive region in a semiconductor device, comprising the steps of:

forming a trench, in which a width of a bottom is wider than a top, in a given region of a semiconductor substrate; and

burying the trench with an insulating layer while forming empty spaces at both corners of the bottom of the trench, by using a coverage characteristic of an insulating material.

2. The method for claim 1, wherein the step of forming the trench comprises the steps of:

forming a mask pattern on the semiconductor substrate;

etching the semiconductor substrate to a given depth by means of a first etch process, thus forming the trench;

forming the trench to a target depth by means of a second etch process in a vertical and a horizontal directions, while forming the trench to have the bottom wider than the top in width; and

removing the mask pattern.

3. The method for claim 2, wherein upon the first etch process, polymer is deposited on the sidewall of the trench while being generated, thus serving as an anti-etch film at the time of the second etch process.

4. The method for claim 3, wherein the first etch process is performed by applying a power in the range of 300W to 2000W in an RIE reactor and using an etch gas containing chlorine.

5. The method for claim 3, wherein the second etch process uses a mixed solution of HNO_3:HF:H_2O as an etchant.

6. The method for claim 3, wherein the first etch process and the second etch process are performed repeatedly to form the trench to a target depth.

7. The method for claim 2, wherein the first etch process is performed using a dry etch process and the second etch process is performed using a wet etch process.

8. The method for claim 7, wherein the first etch process is performed by applying a power in the range of 300W to 2000W in an RIE reactor and using an etch gas containing chlorine.

9. The method for claim 7, wherein the second etch process uses a mixed solution of HNO_3:HF:H_2O as an etchant.

10. The method for claim 7, wherein the first etch process and the second etch process are performed repeatedly to form the trench to a target depth.

11. The method for claim 2, wherein the first etch process is performed by applying a power in the range of 300W to 2000W in a RIE reactor and using an etch gas containing chlorine.

12. The method for claim 11, wherein the first etch process and the second etch process are performed repeatedly to form the trench to a target depth.

13. The method for claim 2, wherein the second etch process uses a mixed solution of HNO_3:HF:H_2O as an etchant.

14. The method for claim 13, wherein the first etch process and the second etch process are performed repeatedly to form the trench to a target depth.

15. The method for claim 2, wherein the first etch process and the second etch process are performed repeatedly to form the trench to a target depth.

16. The method for claim 1, wherein the insulating layer is formed using a TEOS oxide film and is deposited by means of a chemical vapor deposition method under a temperature in the range of 300℃ to 500℃ in a CVD reactor, whereby the insulating layer is not formed at both corners of the bottom of the trench due to a coverage characteristic while being buried into the trench.

17. The method for claim 1, wherein the insulating layer is formed using a SOD or SOG oxide film and is buried into the trench, while the insulating layer is not formed at both corners of the bottom of the trench due to a coverage characteristic of a spin coating oxide film.

18. The method for claim 1, before the trench is buried, further comprising the step of depositing a SiN thin film on the substrate including an inner surface of the trench.